ABSTRACT OF THE DISCLOSURE

In one embodiment, the invention is directed to a general purpose performance counter ("GPPC") connected to a bus carrying debug data. The GPPC comprises an AND/OR circuit connected to receive the debug data; a counter circuit connected to receive from the AND/OR circuit an increment signal that, when activated, causes the counter circuit to increment a count; and a compare circuit for activating a match/threshold signal to the AND/OR circuit responsive to a selected block of the debug data having a first relationship to a compare value, wherein the AND/OR circuit activates the increment signal responsive to a selected combination of bits of an events signal being set.